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An Efficient Digital Baseband Encoder for Short Range Wireless Communication Applications

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Abstract: Various physical layer protocols are employed to encode information bits in short range wireless communication technologies. In this paper, we propose a multimode hardware architecture for a digital baseband encoder which incorporates Manchester, Differential Manchester and FM0 codes. These codes help in achieving good DC balance thereby improving signal reliability. Alternating Manchester with Differential Manchester for different intervals of time improves security at the physical layer level. This work aims at efficient integration of hardware components for the three coding modes.

Keywords: Manchester; Differential Manchester; FM0; Short range wireless communication; VLSI.

I. INTRODUCTION

Short range wireless communication systems have become ubiquitous in our day to day life. To name a few, Wi-Fi Zigbee, Bluetooth, RFID, UWB etc. have worked wonders in several fields including security, medical care, vehicular communication and consumer applications. These technologies employ different physical layer protocols for encoding the information bits. Different standards support different encoding mechanisms. These include Manchester encoding, Differential Manchester encoding and FM0 encoding. These come under the category of bi-phase codes. They have a signal transition within a bit duration thus providing adequate timing information to the receiving end. They have good DC balance – equal number of 1's and 0's throughout a message frame irrespective of its content. Manchester encoding is the simplest of these coding mechanisms and has a lower probability of error compared to other codes [1], [2]. Differential Manchester coding may appear to be superficially the same as Manchester encoding. Unless we know which code is being used, we cannot determine the encoding just by examining the data. FM0 encoding is otherwise known as bi-phase space encoding [3]. In this paper, we modify the existing architecture for FM0/Manchester encoding in [4] to incorporate Differential Manchester code. It focuses on efficient allocation of hardware components to perform the three encoding operations with maximum hardware utilization. This architecture can be used in applications where the system has to switch between different encoding schemes. Having a separate circuit for each encoding method would consume more resources.

II. RELATED WORK

Different types of baseband coding schemes have been in practice for improving performance of communication systems. Here, the discussion is restricted to digital systems. Manchester, Differential Manchester and FM0 Codes are commonly used in short range communication systems like RF. The encoded signals have good DC balance. A signal is said to be more reliable if it has good DC balance.

Combining the use of Manchester and Differential Manchester for different intervals in the same data sequence facilitates data protection [2]. A key will be used to specify the type of encoding used.

In [5], hardware reused architecture for FM0/Manchester encoder is proposed. The original unbalance type architecture has a poor hardware utilization rate (HUR) of 50%. A modified architecture is proposed which balances the computation load between Manchester and FM0. This technique simplifies the Boolean expressions to have common terms. It achieves a hardware utilization rate to 90%.

In [4], the FM0/Manchester encoder of [5] is improved to achieve 100% HUR. Retiming and logic sharing techniques are used to obtain improvement. This architecture is fully reusable and offers competitive performance when compared with other previous works.

Reference [6] proposes a fully reused FM0/Manchester codec for dedicated short range communication (DSRC) based sensor nodes. It has 100% hardware utilization and reduced number of transistors. However, power consumption becomes a tradeoff for HUR.

In [7], the authors propose a modified Manchester/Miller encoder for RFID applications. It has a simple circuit structure and is capable of operating at high frequency. Hardware sharing is adopted to reduce the number of

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transistors. Parallelized operation is used to increase the data throughput. In [8], an FSM based Manchester encoder is designed for use in UHF RFID tag emulator. This design is efficient in terms of area and speed. Reference [9] presents FSM based design of FM0 and Miller encoders for UHF RFID tag emulators.

III. A REVIEW OF CODING SCHEMES

A. Manchester Encoding

Manchester encoding always has a transition in the middle of a bit: a positive transition for an input '1' and a negative transition for an input '0'. This can be obtained by an XOR operation between the input, X and Clock.
Manchester= X XOR Clock

B. Differential Manchester Encoding

Differential Manchester encoding is a modification of Manchester encoding. Both appear to be the same, except for a difference in transitions at the edge of a bit window. There is a transition between windows for an input '0' and there is no transition for an input '1'.The expressions for Differential Manchester encoding are obtained using FSM approach. The state diagram is shown in Fig. 1 and the state transition table is shown in Table I. A and B denote the positive half cycle and negative half cycle parts of the code for a single input.
$A^+ = x \wedge a$
$B^+ = \sim(x \wedge a)$
Where A^+ and B^+ are next state values of A and B respectively.
diff_manch = (clock*A^+) + ((~clock)*B^+)

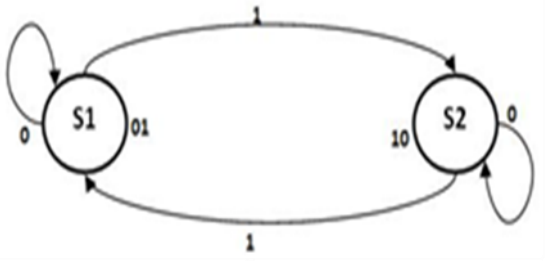

Fig. 1. State diagram for differential Manchester

Current State			Next State					
	A	B	X=0	A +	B+	X=1	A+	B+
S1	0	1		0	1		1	0
S2	1	0		1	0		0	1

Table 1 State transition table for Differential Manchester

C. FM0 Encoding

In the FM0 code, when the input bit is '0' there is a transition in the middle of the bit window, whereas there is no mid bit transition for an input '1'. However, there is a transition at the edge of every bit window. The state diagram for FM0 code is shown in Fig. 2 and the state transition table is shown in Table II.

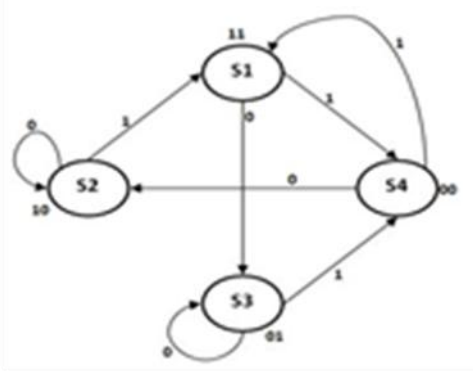

Fig. 2: State diagram for fm0 encoder

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Similar to Differential Manchester encoding, the expressions for FM0 encoding are derived as follows:
$A^{+}=(\sim b)$
$B^{+}=(x \wedge b)$
$fm0 =(clock*A^{+})+((\sim clock)*B^{+})$

Current State			Next State					
	A	B	X=0	A+	B+	X=1	A+	B+
S1	1	1		0	1		0	0
S2	1	0		1	0		1	1
S3	0	1		0	1		0	0
S4	0	0		1	0		1	1

Table 2: State transition table for fm0

IV. PROPOSED WORK

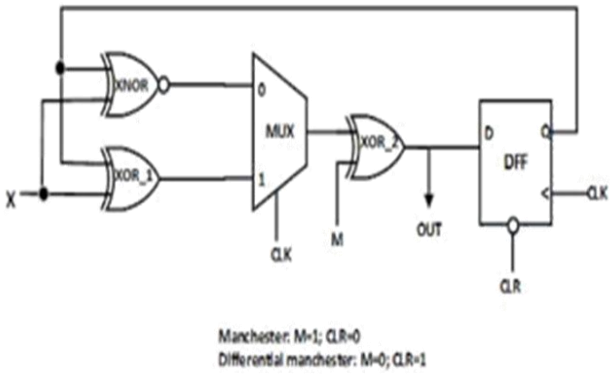

Fig 3: Proposed Differential Manchester circuit

Fig.3 shows the proposed encoding architecture for Manchester / Differential Manchester code. The D flip flop (DFF) stores the current state of A. The MUX selects the next state values of A or B according to the Clock. A mode signal, M and a flip flop clear signal (active low), CLR are used to select between Manchester and Differential Manchester encodings. In Manchester mode, CLR is enabled which feeds a '0' in the place of current value of A and M = 1 which makes XOR_2 act as an inverter. In Differential Manchester mode, CLR=1 and M=0. The current value of A is passed as input to the next state. XOR_2 acts as a buffer.

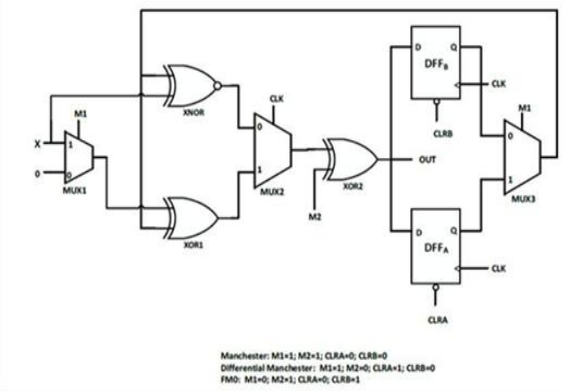

Fig. 4: Proposed multimode encoder architecture

Further, to include FM0 encoding, the architecture is modified as shown in Fig.4. It has a dual bit mode signal – M1, M2 and clear signals – CLRA and CLRB for the two flip flops DFFA and DFFB. CLRA and CLB are active low. Based on different combinations of the signals, the circuit is switched between different modes of operation. DFFA

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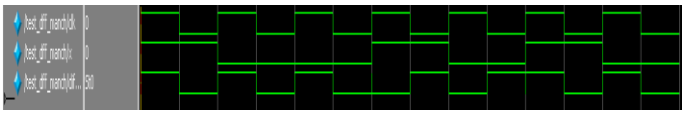
stores the current value of A and DFFB stores the current value of B. DFFA is negative edge triggered and DFFB is positive edge triggered. MUX_3 selects the value of A or B to be as input for next state according to the value of M1. FM0 needs the previous value of B and Differential Manchester / Manchester needs the previous value of A. However, for Manchester, the value of A becomes '0' by enabling CLRA. MUX_1 selects a '0' forFM0 encoding and the value of input X otherwise. The '0' for MUX_1 can also be fed by connecting it to the output of DFFA.

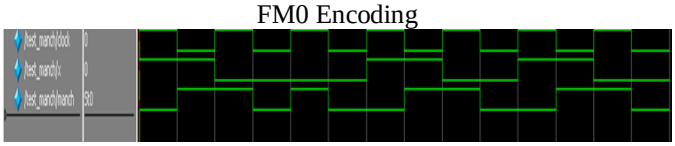
V. RESULTS AND ANALYSIS

The proposed architecture has been implemented in Xilinx Fig.5 shows the simulation waveforms for all the three modes. Results are shown in Table.III. Comparisons with show that our work supports an added Differential Manchester coding mode with a slight increase in resource usage. This increase in area and power is acceptable since our work supports Differential Manchester encoding also. Including this encoding scheme improves the data protection features of the system at the physical layer level. This design gave satisfactory results when tested on board.
This work focuses on efficient integration of Manchester/Differential Manchester/ FM0 coding modes on a single hardware architecture. FM0 and Differential Manchester coding are complex when compared to Manchester coding. Hence the operating frequency of Manchester will be limited by the other 2 modes, which will be higher otherwise.



Differential Manchester Encoding

FM0 Encoding



Manchester Encoding

Fig. 5. Simulation Waveforms

Logic Utilization	Manchester	Fm0	Differential	Multi mode
Number of slice LUTs	1	3	3	4
Number of fully used LUT-FF pairs	0	0	0	0
Number of bonded IOBs	3	3	3	8
Number of DSP-LBE	-----	2	2	-----
Number of slice registers	-----	-----	------	2
Number of BUFG	-----	-----	-----	1

Table 3: Performance analysis

VI. CONCLUSION

This work presents a fully integrated VLSI architecture for Manchester, Differential Manchester and FM0 encoding schemes. These encoding schemes are used in short range communication systems for improving signal reliability. The original Differential Manchester encoder is slightly modified to include Manchester encoding capability. Further, a few more components are added so that the final architecture includes the functionality of FM0 code. This design is compared with the existing integrated architecture of FM0/Manchester codes. Power consumption has increased by 17.24% with a slight increase in area. However the proposed work supports an extra coding mechanism without wasting any logic component. This architecture can be used in applications where the system has to switch between different encoding schemes.

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